REMARKS

The Examiner is thanked for the indication that claims 9 and 31 are directed to allowable subject matter. Applicants have rewritten claims 9 and 31 in independent form as new claims 39 and 40, respectively.

Claims 1-33 were examined in the Office Action. Applicants have amended claims 1, 2, 14, 21, and 32; added new claims 34-42; and cancelled without prejudice claims 22, 24-27, 30, and 31. Accordingly, claims 1-21, 23, 28, 29, and 32-42 are presented for consideration.

The Examiner has requested a copy of relevant pages from the Kline reference. The reference is only 8 pages long, so Applicants have included a copy of the entire reference and direct the examiner to the entire reference as being relevant, with pages 5, 6, and 8 having been pointed out to Applicant's representative as possibly being more relevant.

In response to the Examiner's objection to the sentence on page 44, lines 23-24, Applicants have amended the sentence.

Claims 1, 3-5, 8, and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson (4,463,612) in view of Rozenblit et al. (6,466,069) and further in view of Ims (3,751,979). Applicants respectfully disagree, and explain below that there is no motivation to combine these references. However, to expedite prosecution Applicants have amended claim 1 to more clearly recite the invention. Accordingly, Applicants respectfully submit that the rejection has been overcome by the arguments below, or is moot in light of the amendments.

Applicants submit that the there is no motivation to combine Rozenblit et al. with Thompson. Rozenblit et al. describe a process in which (i) a PLL is in a slow mode having a small bandwidth, (ii) a signal is received at the PLL indicating that a frequency change is desired, (iii) the PLL is put into a fast mode having a large bandwidth, (iv) the frequency is changed, and (v) the PLL is put back into the slow mode (col. 5, lines 58-67). Rozenblit et al. teach the use of a "change bandwidth signal 130" to indicate whether the slow mode or the fast mode is desired, and to cause the PLL to move into the desired mode. In the process outlined above, the "change bandwidth signal" is changed before the frequency changes. See, for example, (i) col. 5, lines 59-61, stating that the "change bandwidth signal switches . . . indicating

a change in the bandwidth . . . is desired" (emphasis added), and (ii) col. 8, lines 21-25 (and Fig. 3), stating that "a change in the desired frequency . . . is detected. For example, a control signal may be received that indicates a change in the desired frequency" (emphasis added). By switching the "change bandwidth signal" before changing frequency, the PLL is allowed to move out of the slow mode (see col. 5, lines 29-32) before the frequency begins to change, so that the PLL can track the frequency in the fast mode when the frequency does change. Rozenblit et al. do not disclose or suggest switching the "change bandwidth signal" after the frequency has started changing.

Thompson describes a single PLL and does not describe or suggest changing the characteristics of the PLL. The PLL of Thompson is used to track a vortex frequency signal that changes unexpectedly (see, e.g., col. 3, lines 14-15 and 24-30). As a result, Thompson would be unable to provide a signal to the PLL of Rozenblit et al. to indicate that a frequency change was about to occur.

Applicants further submit that, even if Rozenblit et al. could be properly combined with Thompson, there would be no motivation to add Ims to such a combination.

Ims describes a PLL-based system that operates on two separate input signals. Ims describes an embodiment that uses a single PLL 68 to alternately lock onto two separate input signals that have different, but constant, frequencies (col. 6, lines 25-40; Fig. 5; see also col. 16, lines 55-56). Ims also describes an alternate embodiment that uses two separate but identical PLLs 68 operating simultaneously on the two separate input signals having different, but constant, frequencies (col. 16, lines 6-37 and 55-56; Fig. 8). In the alternate embodiment, Ims teaches that a "switch 208 . . . alternately [applies] the outputs of the two phase locked loops 68 to the computation unit 70" (col. 16, lines 26-28).

The Office Action cites to column 16, lines 54-56 for support for the assertion that the combination of Thompson and Rozenblit et al would be more efficient if Ims were added. Applicants disagree. Ims does state that its two-PLL embodiment is more efficient than its single-PLL embodiment. However, the increased efficiency arises because "each phase locked loop 68 [in the two-PLL embodiment] operates continuously at one frequency," whereas the

single-PLL embodiment must "allow the PLL 68 time to reacquire the upstream and downstream frequencies," which are different, after switching between the two input signals. Such a gain in efficiency would not arise if two PLLs were used in Rozenblit et al. because Rozenblit et al. do not need to wait for the signal to be reacquired when switching between modes. Rather, Rozenblit et al. operate on a single input signal that remains in an acquired state as the PLL is switched between modes.

The Office Action also asserts the combination of Thompson and Rozenblit et al. would be "faster" and "simpler" if Ims were added, but the Office Action offers no citation to support this assertion. Applicants disagree. Rozenblit et al. teach that the PLL switches to the fast mode "rapidly," that "the charge pump 104 can switch rapidly to the fast and the slow mode," and that the "switching speed can be adjusted" (col. 5, lines 31-40). There is no support for the assertion that switching between PLLs, as in Ims, would be "faster." Regarding the "simpler" assertion, Rozenblit et al. switch modes using a single signal (the "change bandwidth signal") and using a single PLL. There is no support for the assertion that using two separate PLLs would be simpler. Additionally, switching between two separate PLLs would presumably introduce switching noise that would need to be filtered out or otherwise addressed.

Accordingly, for at least these reasons Applicants submit that a *prima facie* case of obviousness has not been established with respect to claims 1, 3-5, 8, and 13.

Applicants further submit that this rejection is moot in light of the amendment to claim 1. For example, neither Thompson, Rozenblit et al., or Ims disclose or suggest at least the following recitation from claim 1:

> a switch operable to switch an output signal of the process variable transmitter between the first output signal and the second output signal in response to a change in the frequency, and based on at least one of a first lock indicator signal and a second lock indicator signal, wherein the first lock indicator signal indicates whether the first phase-locked loop is locked into the frequency and the second lock indicator signal indicates whether the second phase-locked loop is locked into the frequency.

Rather, as noted by the Office Action, Thompson describes only a single PLL and therefore does not describe the recited switch.

Rozenblit et al. describe changing the bandwidth of a single PLL using the "change bandwidth signal" as a control signal (col. 8, lines 21-25). The control signal reflects a desire to change the frequency (see, e.g., col. 5, lines 59-61; col. 8, lines 21-25; Fig. 3) and not a "response to a change in the frequency" as recited.

Ims describes the use of two separate but identical PLLs 68 (see Fig. 8 and col. 16) operating on different signals having constant, but different, frequencies. "A switch 208 . . . alternately [applies] the outputs of the two phase locked loops 68 to the computation unit 70" (col. 16, lines 26-28). Switch 208 alternates between the two phase locked loops 68 merely to receive information from both and not "in response to a change in the frequency, and based on at least one of [multiple] lock indicator signal[s]" as recited.

Finally, Applicants note that Rozenblit et al. do not describe changing bandwidth "upon a determination that the phase locked loop is locked," as the Office Action appears to suggest (see Office Action at 4, citing column 4, lines 28-32). Rather, the cited passage of column 4, lines 28-32 indicates how to determine if the PLL is locked, but does not suggest changing bandwidth based on the PLL being in lock. To the contrary, Rozenblit et al. teach that changing bandwidth is based on a desire to change the frequency of the input signal, or on the desired change having been accomplished (see col. 5, lines 58-67; col. 8, lines 21-25; Fig. 3); presumably each of these scenarios involves the PLL being in lock prior to the desired change, and staying in lock during and after the change.

Accordingly, for at least these reasons, claim 1 and the claims that depend therefrom (including claims 3-5, 8, and 13) are patentable over the applied references.

Claims 14-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit et al. and Ims and further in view of Vignos et al. (5,576,497). Applicants respectfully disagree because, as explained above there is no motivation to combine at least Thompson, Rozenblit et al., and Ims. However, to expedite prosecution Applicants have amended claim 14 to more clearly recite the invention. Accordingly, Applicants respectfully submit that the rejection has been overcome by the arguments above, or is moot in light of the amendments.

Applicants submit that this rejection is moot in light of the amendment to claim 14. For example, neither Thompson, Rozenblit et al., Ims, or Vignos et al. disclose or suggest at least the claim 14 limitation of a signal processor comprising:

> a switch for switching the output signal generated by the signal processor from among the PLL output signals in response to a change in the frequency, and based on one or more lock indicator signals, wherein the one or more lock indicator signals each indicate whether a corresponding phase-locked loop is locked onto the flow sensor signal.

Rather, Thompson describes only a single PLL and therefore does not describe the recited switch. Rozenblit et al. describe changing the bandwidth of a PLL using a control signal that reflects a desire to change the frequency and is not "in response to a change in the frequency, and based on one or more lock indicator signals" as recited. Ims describes a switch 208 that alternates between two phase locked loops 68 merely to receive information from both and not "in response to a change in the frequency, and based on one or more lock indicator signals" as recited. Vignos et al. does not describe a PLL or the recited switch, but, rather, describes an adaptive filter 35 for filtering a signal originating from a vortex sensor (see col. 4, lines 11-32 and Figs. 1-2).

Accordingly, for at least these reasons, Applicants submit that a *prima facie* case of obviousness has not been established with respect to claim 14 and the claims that depend therefrom (including claims 15-20), and, in the alternative, that such claims are patentable over the applied references.

Applicants have rewritten claim 20 in independent form (without the amendment to claim 14) as new claim 38, and submit that claim 38 is patentable over the applied combination of Thompson, Rozenblit et al., Ims, and Vignos. In rejecting claim 20, the Office Action asserts that "Vignos also teaches that the pre-filtering is switched on and off based upon high or low flow signals obtained in accordance with filter cut-off frequencies (column 2, lines 58-67 and column 6, lines 25-37)" (Office Action at 6). Applicants respectfully disagree. Claim 38 recites in part, and Vignos fails to disclose or suggest at least, that "the filter is switchable between an ON state and an OFF state, and is switched to the ON state based on the low flow signal."

Rather, Vignos describes a filter that is always on, with the high and low cut-off frequencies being adjusted based on the frequency (see col. 2, lines 58-67) and the rate of change of the frequency (see col. 11, lines 6-30). The passage at col. 6, lines 25-37 describes upper thresholds on the high cut-off frequency for the bandpass filter of Vignos. For at least these reasons, Applicants submit that a *prima facie* case of obviousness has not been established with respect to claims 38 and, in the alternative, that claim 38 is patentable over the applied references.

Claims 2, 21, 22, 24, and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit et al. and Ims and further in view of Olgaard (6,236,278). Applicants respectfully disagree because, as explained above there is no motivation to combine at least Thompson, Rozenblit et al., and Ims. However, to expedite prosecution Applicants have amended claim 21, as well as claim 1, to more clearly recite the invention. Accordingly, Applicants respectfully submit that the rejection has been overcome by the arguments above, or is moot in light of the amendments.

With respect to claim 2, Applicants note that claim 2 depends from claim 1 and submit that Olgaard does not overcome the deficiencies of Thompson, Rozenblit et al., and Ims. For example, Olgaard does not disclose or suggest at least the following recitation from claim 1:

> a switch operable to switch an output signal of the process variable transmitter between the first output signal and the second output signal in response to a change in the frequency, and based on at least one of a first lock indicator signal and a second lock indicator signal, wherein the first lock indicator signal indicates whether the first phase-locked loop is locked into the frequency and the second lock indicator signal indicates whether the second phase-locked loop is locked into the frequency

Rather, Olgaard, as with Thompson, describes only a single PLL and therefore does not describe the recited switch. Applicants further note that although Olgaard may describe modifying a feedback loop from an initial configuration to an operational mode, Olgaard does not describe modifying the feedback from the operational mode to the initial configuration.

With respect to claim 21, none of the applied references disclose or suggest at least the following recitation from claim 21:

> switching the output of the signal processor from the output signal of the second PLL to the output signal of the first PLL when the lock indicator signal indicates that the second PLL is out of lock with the frequency of the input signal

Rather, Thompson and Vignos describe only a single PLL and therefore do not describe the recited switching. Rozenblit et al. describe changing to a higher bandwidth before the frequency changes and, as a result, before the PLL would go out of lock and before a "lock indicator signal indicates that the second PLL is out of lock" as recited. Ims describes switching between PLL outputs in order to sample both outputs and does not describe "switching … from the output signal of the second PLL … when the lock indicator signal indicates that the second PLL is out of lock" as recited.

Accordingly, for at least these reasons, Applicants submit that a *prima facie* case of obviousness has not been established with respect to claims 2 and 21 and the claims that depend therefrom (claims 22, 24, and 29 depend from claim 21), and, in the alternative, that such claims are patentable over the applied references.

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit et al. and Ims and further in view of Bouillet (6,298,100). Applicants respectfully disagree because, as explained above there is no motivation to combine at least Thompson, Rozenblit et al., and Ims. Further, Applicants note that claims 6 and 7 depend from claim 1 and submit that Bouillet does not overcome the deficiencies of Thompson, Rozenblit et al., and Ims with respect to claim 1. For example, Bouillet does not disclose or suggest at least the following recitation from claim 1:

> a switch operable to switch an output signal of the process variable transmitter between the first output signal and the second output signal in response to a change in the frequency, and based on at least one of a first lock indicator signal and a second lock indicator signal, wherein the first lock indicator signal indicates whether the first phase-locked loop is locked into the frequency and the second lock indicator signal indicates whether the second phase-locked loop is locked into the frequency

Rather, Bouillet describes a single-PLL system and, therefore, does not describe the recited switch. Accordingly, for at least these reasons, Applicants submit that a *prima facie* case of obviousness has not been established with respect to claims 6 and 7 and, in the alternative, that such claims are patentable over the applied references.

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit et al. and Ims and further in view of Henry et al. (5,570,300). Applicants respectfully disagree because, as explained above there is no motivation to combine at least Thompson, Rozenblit et al., and Ims. Further, Applicants note that claims 10-12 depend from claim 1 and submit that Henry et al. do not overcome the deficiencies of Thompson, Rozenblit et al., and Ims with respect to claim 1. For example, Henry et al. do not disclose or suggest at least the following recitation from claim 1:

> a switch operable to switch an output signal of the process variable transmitter between the first output signal and the second output signal in response to a change in the frequency, and based on at least one of a first lock indicator signal and a second lock indicator signal, wherein the first lock indicator signal indicates whether the first phase-locked loop is locked into the frequency and the second lock indicator signal indicates whether the second phase-locked loop is locked into the frequency

Rather, Henry et al. describe self-validating sensors and do not describe a system having multiple PLLs and, therefore, do not describe or suggest the recited switch. Accordingly, for at least these reasons Applicants submit that a *prima facie* case of obviousness has not been established with respect to claims 10-12 and, in the alternative, that such claims are patentable over the applied references.

Claims 25-27, 30, 32, and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit et al., Ims, and Olgaard, and further in view of Henry et al. Applicants respectfully disagree because, as explained above there is no motivation to combine at least Thompson, Rozenblit et al., and Ims. However, to expedite prosecution, Applicants have cancelled claims 25-27 and 30, and have amended claims 32 and 33 to more clearly recite the invention. Accordingly, Applicants respectfully submit that the rejection has been overcome by the arguments above, or is moot in light of the amendments.

None of the applied references disclose or suggest at least the following recitation from claim 32:

> the uncertainty value is based on an uncertainty of a frequency of the sinusoidal output signal

Rather, Thompson, Rozenblit et al., Ims, and Olgaard describe PLL-based systems, but do not describe or suggest self-validating sensors or uncertainty values. Henry et al. describe self-validating sensors, as well as applications of self-validating sensors to particular systems, but Henry et al. do not describe the application of self-validating sensors to a PLL-based vortex flow meter as recited. In particular, Henry et al. do not describe at least that an uncertainty value relating to a flow rate output signal "is based on an uncertainty of a frequency of the sinusoidal output signal" as recited. Further, and as a result, Henry et al. do not describe the further recitation from claim 33 that "the uncertainty of the frequency of the sinusoidal output signal is based on an estimate of a variance of the frequency of the sinusoidal output signal." Accordingly, for at least these reasons Applicants submit that a *prima facie* case of obviousness has not been established with respect to claim 32 and claims that depend therefrom (including claim 33) and, in the alternative, that such claims are patentable over the applied references.

Claim 23 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit et al., Ims, and Olgaard, and further in view of Yatsuzuka et al. (5,128,625). Applicants respectfully disagree because, as explained above there is no motivation to combine at least Thompson, Rozenblit et al., and Ims. Further, Applicants note that claim 23 depends from claim 21 and submit that Yatsuzuka et al. do not overcome the deficiencies of Thompson, Rozenblit et al., Ims, and Olgaard with respect to claim 21. For example, Yatsuzuka et al. do not disclose or suggest at least the following recitation from claim 21:

> switching the output of the signal processor from the output signal of the second PLL to the output signal of the first PLL when the lock indicator signal indicates that the second PLL is out of lock with the frequency of the input signal

Rather, Yatsuzuka et al. describe a PLL-based system that uses a training mode to determine an initial phase and center frequency to be used by the PLL during an operational mode. However,

Yatsuzuka et al. do not describe switching between two PLLs as recited. Accordingly, for at least these reasons Applicants submit that a *prima facie* case of obviousness has not been established with respect to claim 23 and, in the alternative, that claim 23 is patentable over the applied references.

Claim 28 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Thompson in view of Rozenblit et al., and Ims, and further in view of Yatsuzuka et al. Applicants respectfully disagree because, as explained above there is no motivation to combine at least Thompson, Rozenblit et al., and Ims. Further, Applicants note that claim 28 depends from claim 1 and submit that Yatsuzuka et al. do not overcome the deficiencies of Thompson, Rozenblit et al., and Ims with respect to claim 1. For example, Yatsuzuka et al. do not disclose or suggest at least the following recitation from claim 1:

> a switch operable to switch an output signal of the process variable transmitter between the first output signal and the second output signal in response to a change in the frequency, and based on at least one of a first lock indicator signal and a second lock indicator signal, wherein the first lock indicator signal indicates whether the first phase-locked loop is locked into the frequency and the second lock indicator signal indicates whether the second phase-locked loop is locked into the frequency

Rather, Yatsuzuka et al. describe a PLL-based system that uses a training mode to determine an initial phase and center frequency to be used by the PLL during an operational mode. However, Yatsuzuka et al. do not describe a switch for switching between two PLLs as recited. Accordingly, for at least these reasons Applicants submit that a *prima facie* case of obviousness has not been established with respect to claim 28 and, in the alternative, that claim 28 is patentable over the applied references.

Applicants disagree with certain of the Office Action's characterizations of the cited references but, for clarity and brevity in argument, have generally not addressed such characterizations unless required by the line of reasoning in the above arguments. Accordingly, Applicants' silence should not be construed as acquiescing in any of the Office Action's characterizations of the cited references.

Please apply the $132 check for excess claim fees and any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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